-- REMARKS --

Claims 9-13. In the Final Office Action, Examiner Shapiro rejected pending claims 9-13 on various grounds. The Applicant responds to each rejection as subsequently recited herein, and respectfully requests reconsideration of the present application:

A. Examiner Shapiro rejected pending claim 13 under 35 U.S.C. §102(e) as being anticipated by U.S. Patent No. 6,384,806 to *Matsueda* et al.

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of independent claim 13 over *Matsueda*. The Applicant has also thoroughly re-read *Matsueda*. To warrant this anticipation rejection, *Matsueda* must show each and every element set forth in independent claim 13 in as complete detail as is contained in independent claim 13. See, MPEP §2131. The Applicant respectfully traverses this anticipation rejection of claim 13, because *Matsueda* fails to disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein an order in which said signal processing circuits are arranged physically on said substrate is at least partially different than a physical order of said signal bus lines to which said signal processing circuit blocks are respectively connected" as recited in independent claim 13.

As to the traversal, the plurality of signal processing circuits as encompassed by independent claim 13 are directed to the signal processing circuits for providing the 6 bit signal bus line to multiplexing circuit 101 of *Matsueda* (FIG. 15), for providing the 8 bit signal bus line to multiplexing circuit 101' of *Matsueda* (FIG. 16), and for providing signal bus lines D1B-DuB and D1T-DuT to multiplexing circuits 101A and 101B, respectively, of *Matsueda* (FIG. 17). These signal processing circuits are not illustrated in FIGS. 15-17 of *Matsueda*, and more

importantly, *Matsueda* fails to provide any teachings related to the physical order of these signal processing circuits on the substrates for supporting circuits 101, 101', 101A and 101B.

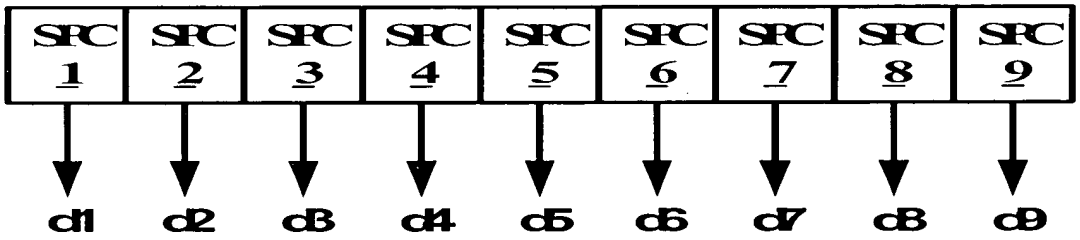
Matsueda unequivocally fails to teach the last limitation of independent claim 13. Withdrawal of the rejection of independent claim 13 under 35 U.S.C. §102(e) as being anticipated by *Matsueda* is therefore respectfully requested.

B. Examiner Shapiro rejected pending claims 9, 10 and 12 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Matsueda* et al. in view of U.S. Patent No. 5,892,493 to *Enami* et al.

The Applicant has thoroughly considered Examiner Shapiro's remarks concerning the patentability of claims 9, 10 and 12 over *Matsueda* in view of *Enami.* The Applicant has also thoroughly re-read *Matsueda* and *Enami.* To warrant this 35 U.S.C. §103(a) rejection of claims 9, 11 and 12, all the claim limitations recited in independent claim 9 must be taught or suggested by the combination of *Matsueda* and *Enami.* See, MPEP §2143. The Applicant respectfully traverses this §103(a) rejection of claims 9, 10 and 12, because neither *Matsueda* nor *Enami* disclose, teach or suggest "a plurality of signal processing circuits integrated on said substrate, each signal processing circuit being connected to a respective bus line, wherein a first signal processing circuit associated with a first address conductor of a first group of address conductors and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on said substrate" as recited in independent claim 9.

As to the traversal, Examiner Shapiro has correctly recognized *Matsueda*'s failure to teach or suggest the last limitation of independent claim 9. However, Examiner Shapiro has erroneously interpreted *Enami* as teaching the last limitation of independent claim 9, because a proper reading of *Enami* reveals that *Enami* also fails to teach or suggest the last limitation of independent claim 9.

Specifically, the last limitation of independent claim 9 is each individual signal processing circuit being associated with a first address conductor of a first group and a last address conductor of a second group are adjacent on the substrate. This limitation is neither taught nor suggested by *Enami* by the disclosure of an order in which the signal processing circuits of data line driver 40 are arranged physically on the substrate in exactly the same physical order of the signal bus lines to which the signal processing circuit blocks of data line driver 40 are respectively connected as evidenced by the following illustration of data line driver 40, wherein n = 9 for nine (9) signal processing circuits SPC1-SPC9 and nine (9) signal bus lines d1-d9.



This is identical to the teachings of the prior art illustrated in FIG. 3 of the present application. Thus, *Enami* is nothing more than a cumulative reference as to teaching an order in which signal processing circuits are arranged physically on the substrate in exactly the same physical order of the signal bus lines to which the signal processing circuit blocks are respectively connected.

In the Final Office Action, Examiner Shapiro misreads the multiplexing circuit 38 of *Enami* (FIGS. 1 and 5) as teaching the last limitation of independent claim 9, and misreads the Applicant's argument dated June 10, 2003, in response to a 35 U.S.C. §112, ¶1 rejection of independent claim 9 as supporting an anticipation of *Enami* of the last limitation on independent claim 9.

The Applicant hereby respectfully clarifies that the last limitation of independent claim 9 is directed to a physical order of the signal processing circuits within the data line driver 40 of *Enami* (FIGS. 1 and 5) by which signal processing circuits of data line driver 40 are not arranged physically on the substrate in exactly the same physical order of the signal bus lines d1...dn to which the signal processing circuit blocks of data line driver 40 are respectively connected. However, *Enami* teaches the signal processing circuits of data line driver 40 are arranged physically on the substrate in exactly the same physical order of the signal bus lines d1...dn to which the signal processing circuit blocks of data line driver 40 are respectively connected as set shown herein with the above illustration. *Enami* is clearly synonymous with the FIG. 3 prior art of the present application whereby signal processing circuits 42(1)-42(9) are arranged physically on the substrate in exactly the same physical order of the signal bus lines V1-V9 to which the signal processing circuit blocks 42(1)-42(9) are respectively connected.

Furthermore, the Applicant hereby respectfully clarifies that the June 10, 2003, argument set forth by the Applicant encompasses FIGS. 4 and 5 of the present application whereby signal processing circuits 42(1)-42(9) are not arranged physically on the substrate in exactly the same physical order of the signal bus lines V1-V9 to which the signal processing circuit blocks 42(1)-42(9) are respectively connected to thereby allow, for example, signal processing circuit 42(1) and 42(9) to be adjacent on the substrate.

The combination of *Matsueda* in view of *Enami* unequivocally fails to teach the last limitation of independent claim 9. Withdrawal of the rejection of independent claim 9 under 35 U.S.C. §103(a) as being unpatentable over *Matsueda* in view of *Enami* is therefore respectfully requested.

Claims 10 and 12 depend from independent claim 9. Therefore, dependent claims 10 and 12 include all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claims 10 and 12 are allowable over *Matsueda* in view of *Enami* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Matsueda* in view of *Enami*. Withdrawal of the rejection of dependent claims 10 and 12 under 35 U.S.C. §103(a) being unpatentable over *Matsueda* in view of *Enami* is therefore respectfully requested.

C. Examiner Shapiro rejected pending claim 11 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,384,806 to *Matsueda* et al. in view of U.S. Patent No. 5,892,493 to *Enami* et al. and in further view of U.S. Patent No. 6,144,426 to *Yamazaki* et al.

Claim 11 depends from independent claim 9. Therefore, dependent claim 11 includes all of the elements and limitations of independent claim 9. It is therefore respectfully submitted by the Applicant that dependent claim 11 is allowable over *Matsueda* in view of *Enami* and in further view of *Yamazaki* for at least the same reason as set forth herein with respect to independent claim 9 being allowable over *Matsueda* in view of *Enami*. Withdrawal of the rejection of dependent claim 9 under 35 U.S.C. §103(a) being unpatentable over *Matsueda* in view of *Enami* and in further view of *Yamazaki* is therefore respectfully requested.

SUMMARY

Examiner Shapiro's rejection of claims 9-12 have been obviated by the remarks herein supporting an allowance of pending claims 9-12 over *Matsueda* in view of *Enami*. Examiner Shapiro's rejection of claim 13 has been obviated by the remarks herein supporting an allowance of pending claim 13 over *Matsueda*. The Applicant respectfully submits that claims 9-13 as listed herein fully satisfy the requirements of 35 U.S.C. §§ 102, 103 and 112. In view of the foregoing, favorable consideration and early passage to issue of the present application is respectfully requested. If any points remain in issue that may best be resolved through a personal or telephonic interview, Examiner Shapiro is respectfully requested to contact the undersigned at the telephone number listed below.

Dated: **August 19, 2004**

Respectfully submitted,
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